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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,323	10/09/2003	Joseph A. Yedinak	90065.000431/17732.56390.	9818

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/682,323	**Applicant(s)** YEDINAK ET AL.
	Examiner Thomas L Dickey	**Art Unit** 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,9,10,12,13,18 and 19* is/are allowed.

6)☒ Claim(s) *1-3,5-8,11 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 11/29/2004 has been entered.

Drawings

2. The formal drawings filed on 11/29/2004 are acceptable.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 14-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JOHN M. S. NEILSON (5,382,825).

Neilson discloses an integrated circuit comprising a die having a device layer 12; an insulating/oxide layer (marked SiO_2) disposed over said device layer 12; a die street 14 defining the outer most bounds of said die; a voltage divider network (described at column 2 lines 52-55) including a plurality of resistive elements connected in series to each other, a plurality of predetermined bias voltages derived by said voltage divider network, each of said bias voltages being dependent at least in part upon a corresponding one of said resistive elements; and a field plate termination including a plurality of field plates 34, said field plates 34 disposed on said insulating/oxide layer (marked SiO_2) and being laterally spaced apart relative to each other and relative to said die street 14, each of said plurality of field plates 34 electrically connected to a corresponding one of said plurality of predetermined bias voltages; and a method of distributing an electrical field within an integrated circuit die to thereby increase the breakdown voltage of said integrated circuit, said die having a device layer 12, an insulating/oxide layer (marked SiO_2), and a die street 14 formed on said die, said method comprising the steps of disposing a plurality of field plates 34 on said die, said field plates 34 being spaced apart relative to each other and relative to said die street 14; and resistively dividing a potential difference to generate a plurality of bias voltages, said bias voltages ranging from a relatively low value to a relatively high value; and applying a respective one of said plurality of bias voltages to each of said field plates 34 such that the bias voltage applied to a particular field plate increases with the proximity of that particular field plate to said die street 14, wherein said resistively dividing step comprises electrically connecting a series combination of one or more polysilicon resistors and MOSFET devices between said die street 14 and one of an emitter and gate of said integrated circuit. Note figure 3 and column 2 lines 50-60 of Neilson.

Claims 1-3,5-8 and 11 stand rejected under 35 U.S.C. 102(b) as being anticipated by TADA et al. (6,525,390).

Tada et al. discloses an integrated circuit comprising a die having a device layer, an emitter 203, a collector 201, an insulating/oxide layer 211 disposed over said device layer, a die street 210 defining the outer most bounds of said die, a voltage divider network, 206A-206B-207-208 integral and monolithic with said die, including a plurality of resistive elements/MOSFET devices connected in series to each other to form a serpentine polysilicon resistor 205a-205b electrically connecting said emitter 203 and said collector 201, said resistor 205a-205b having a length, a plurality of predetermined bias voltages derived by said voltage divider network, each of said bias voltages being dependent at least in part upon a corresponding one of said resistive elements; and a field plate termination including a plurality of field plates 205, said field plates 205 disposed on said insulating/oxide layer 211, connected to said resistor 205a-205b at respective points along said length thereof, and laterally spaced apart relative to each other and relative to said die street 210, wherein said polysilicon resistor 205a-205b is uniformly doped along its length to provide a continuous resistance between the emitter 203 and the collector 201, and said voltage divider network includes a combination of MOSFET devices and resistors. Note figures 27(a)-27(b), column 13 lines 45-67, and column 14 lines 1-15 and 25 of Tada et al.

Allowable Subject Matter

4. Claims 4,9,10,12, and 13 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an integrated circuit, comprising a die having a device layer; an insulating layer disposed over said device layer; a die street defining the outer most bounds of said die; a voltage divider network including a plurality of resistive elements connected in series to each other, a plurality of predetermined bias voltages derived by said voltage divider network, each of said bias voltages being dependent at least in part upon a corresponding one of said resistive elements; and a field plate termination including a plurality of field plates, said field plates disposed on said oxide layer and being laterally spaced apart relative to each other and relative to said die street, each of said plurality of field plates electrically connected to a corresponding one of said plurality of predetermined bias voltages, further comprising an emitter and a collector, said voltage divider network comprising a serpentine polysilicon resistor electrically connecting said emitter and said collector, said resistor having a length, said plurality of field plates being connected to said resistor at respective points along said length thereof, wherein said voltage divider network includes MOSFET devices, as recited in claim 4, or wherein said predetermined bias voltage applied to a particular one of said field plates is dependent at least in part upon the proximity of said particular one of said field plates to said die street, and said plurality of field plates comprise a first, second and third field plate, said first field plate being disposed relatively proximate to said die street, said second field plate being disposed between said first and third field plates relative to said die street, and said third field plate being disposed relatively distant from said die street; and said voltage divider network being connected across a potential difference and generating a first, second and third voltage, said first voltage applied to said first field plate and being from approximately fifty to approximately sixty percent of said potential difference, said second voltage applied to said second field plate and being from approximately twenty to approximately thirty percent of said potential difference, and said third voltage applied to said third field plate and being from approximately fifteen to approximately twenty percent of said potential difference, as recited in claim 9, or wherein each of said plurality of field plates has a predetermined and respective width, said widths of said field plates being separately adjusted dependent at least in part upon a voltage rating of said integrated circuit, as recited in claim 12, or wherein each of said plurality of field plates is separated from another of said plurality of field plates by a predetermined and respective distance, said distances being adjusted dependent at least in part upon a voltage rating of said integrated circuit, as recited in claim 13.

Claims 18 and 19 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a method of distributing an electrical field within an integrated circuit die to thereby increase the breakdown voltage of said integrated circuit, said die having a device layer and an insulating layer, a die street formed on said die, said method comprising the steps of: disposing a plurality of field plates on said die, said field plates being spaced apart relative to each other and relative to said die street; and resistively dividing a potential difference to generate a plurality of bias voltages, said bias voltages ranging from a relatively low value to a relatively high value; applying a respective one of said plurality of bias voltages to each of said field plates such that the bias voltage applied to a particular field plate increases with the proximity of that particular field plate to said die street, said resistively dividing step comprises electrically connecting one or more polysilicon resistors between said die street and one of an emitter and gate of said integrated circuit, and wherein said disposing step comprises disposing first, second and third field plates on said die, said first field plate being relatively proximate to said die street, said second field plate being disposed between said first and second field plates, and said third field plate being disposed relatively distant from said die street; and said applying step comprises applying a first, second and third bias voltage to said first second and third field plates, respectively, said first bias voltage having a value of from approximately fifty to approximately sixty percent of said potential difference, said second bias voltage having a value of from approximately twenty to approximately thirty percent of said potential difference, and said third bias voltage having a value of from approximately fifteen to approximately twenty percent of said potential difference, as recited in claim 18.

Response to Arguments

5. Applicant's arguments filed 11/29/04 have been fully considered but they are not persuasive.

At page 11 of the remarks, after citing a passage[1] of the prior art, Applicant states, "In short, the annular rings of Neilson are biased to the same or equal voltages/ potentials whereas the field plates of the present invention are biased to different voltages/potentials." However, Applicant's statement is not supported by the cited passage. In ordinary usage, the words "equipotential ring" are used to describe a ring that is at a single voltage throughout its own body, not to describe a ring that is at the same voltage as some other object. Further, in ordinary usage, the words "resistors or diodes (not shown) to force voltage to be distributed uniformly from ring-to-ring" describe a network that distributes a different voltage to each of several rings.

It is argued, at page 12 of the remarks, that "In contrast, as discussed above, the rings of Neilsen [sic] are equipotential rings, i.e., each of the rings as the same potential or applied voltage. Thus, Neilson fails to disclose dividing a potential difference to generate a plurality of bias voltages ranging from a relatively low value to a relatively high value and applying a respective one of the plurality of bias voltages to each of the field plates such that the bias voltage applied to a particular field plate increases with the proximity of that field plate to the die street, as recited in part by claim 14." However, as explained above, Applicant misreads the meaning of "equipotential ring." Further, Neilson's words, "connected by resistors or diodes (not shown) to force voltage to be distributed uniformly from ring-to-ring," convey to one skilled in the art that Neilson is describing (as required by 35 USC 102(b)) a device that divides a potential difference to generate a plurality of bias voltages ranging from a relatively low value to a relatively high value and applies a respective one of the plurality of bias voltages to each of the field plates such that the bias voltage applied to a particular field plate increases with the proximity of that field plate to the die street, as required by claim 14.

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[1] "[A]nnular equipotential rings 34 such as illustrated in FIG. 3 ... are connected by resistors or diodes (not shown) to force voltage to be distributed uniformly from ring-to-ring across the edge passivation area 10." Neilson; John M. S., US Patent No. 5382825, column 2, lines 51-54.

It is argued, at page 13 of the remarks, that "Tada, et al., applies a single reverse voltage to the chain of diodes, and an equal voltage is dropped across each diode. The device of Tada, et al., does not generate a plurality of predetermined bias voltages, nor are the diodes connected to corresponding and different predetermined bias voltages." However, applicant admits that a different voltage exists at the two ends of each of diode (the difference being the "equal voltage ... dropped across each diode," note Applicant's remarks at page 13). There are a plurality (Applicant estimates 280, note Applicant's remarks at page 13) of diodes, and thus a plurality of nodes between said diodes, each of said nodes being at a different one (Applicant estimates the difference, as measured between adjacent nodes, to be 2.5 Volts, note Applicant's remarks at page 13) of a plurality of predetermined bias voltages, each field plate 205 being connected to one of said nodes.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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